Task Control Block TCB
Task_ID
Status/Priority
Task_Next_IP_H
Task_Next_IP_M
Task_Next_IP_L
Task_Start_IP_H
Task_Start_IP_M
Task_Start_IP_L
Ready_Wait_Time
Event_ID
Event_Control
Next_TCB_H
Next_TCB_L

Fig.1 - Data Memory – Task Control Block

Task_Information_Block
Task_ID
Pipe_ID
Mutex_ID
Next_TIB_H
Next_TIB_L

Fig 2 - Data Memory – Task Information Block

Event Control Block ECB
Event_ID
Control/Status
Next_ECB_H
Next_ECB_L

Fig 3 - Data Memory – Event Control Block

PIPE Control Block PCB
PIPE_ID
PIPE_Base_Address
PIPE_Size
Next_PCB_H
Next_PCB_L

Fig 4 - Data Memory - Pipe Control Block

Data Memory Control Block DMCB
Task_ID
Data_Memory_Base_Address
Data_Memory_Size
Next_DMCB_H
Next_DMCB_L

Fig 5 - Data Memory – Data Memory Control Block

Task_Data_Memory
Task_ID
REG0
REG1
REGx
DATA0
.
DATAn

Fig 6 - Data Memory – Task Data Memory

Port_Information_Block
Asignation_Port_Mask_A
Asignation_Port_Mask_B
Asignation_Port_Mask_C
Asignation_Port_Mask_D
Asignation_Port_Mask_E
Asignation_Port_Mask_F
.
Input_Selection_Mask_A
Input_Selection_Mask_B
Input_Selection_Mask_C
Input_Selection_Mask_D
Input_Selection_Mask_E
Input_Selection_Mask_F
Idle_State_Mask_A
Idle_State_Mask_B
Idle_State_Mask_C
Idle_State_Mask_D
Idle_State_Mask_E
Idle_State_Mask_F
.
Idle_State_Mask_A
Idle_State_Mask_B
Idle_State_Mask_C
Idle_State_Mask_D
Idle_State_Mask_E
Idle_State_Mask_F
.
Change_State_A
Change_State_B
Change_State_C
Change_State_D
Change_State_E
Change_State_F
.

Fig.7 - Data Memory – Port Information Block

KERNEL control Registers
DM_Remainder_H
DM_Remainder_L
Max_Priority
Max_Wait_Time
Task_ID_Winner
IP_H
IP_M
IP_M
IP_L
DM_Pointer_H
DM_Pointer_L
TCB_Pointer_H
TCB_Pointer_L
ECB_Pointer_H
ECB_Pointer_L
DMCB_Pointer_H
DMCB_Pointer_L
TIB_Pointer_H
TIB_Pointer_L
PCB_Pointer_H
PCB_Pointer_L
Last_TCB_Pointer_H
Last_TCB_Pointer_L
Last_ECB_Pointer_H
Last_ECB_Pointer_L
Last_TIB_Pointer_H
Last_TIB_Pointer_L
Last_PIB_Pointer_H
Last_PIB_Pointer_L
Last_DMCB_Pointer_H
Last_DMCB_Pointer_L

Fig 8 - Data Memory – Kernel Control Registers

Task_Allocation_Table TAT
Task_Condition
Task_Start_IP_H
Task_Start_IP_M
Task_Start_IP_L
Task_Condition
Task_Start_IP_H
Task_Start_IP_M
Task_Start_IP_L
:
.
:
.
Task_Condition
Task_Start_IP_H
Task_Start_IP_M
Task_Start_IP_L

Fig 9 - Program Memory – Task Allocation Table

Task_Header TH
Task_ID
Initial Status/ Priority
Task_Data_Memory_Size
Task Program Code
:
:
:

Fig 10 - Program Memory – Task Header

```
                    ╭─────────────╮
                    │  Dispatcher  │
                    ╰──────┬──────╯
                           │
                           ▼
┌──────────────────────────────────────────────────────┐
│   Port state Update and signaling on port change event │
└──────────────────────────┬─────────────────────────────┘
                           │
                           ▼
          ┌──────────────────────────────┐
          │       Task state Update       │
          └───────────────┬──────────────┘
                           │
                           ▼
          ┌──────────────────────────────┐
          │     Priority task ordering    │
          └───────────────┬──────────────┘
                           │
                           ▼
          ┌──────────────────────────────┐
          │    Context and control restore │
          └──────────────────────────────┘
```
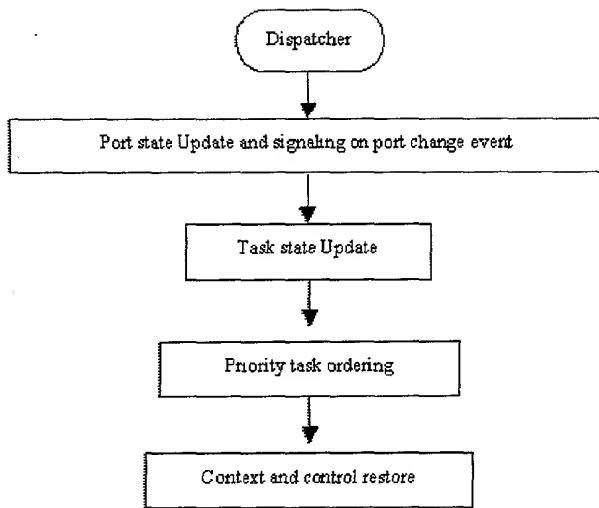
Fig 11 – Kernel – Dispatcher General Flow Chart

```
Port state Update and signaling on port change event
A)          TEMP1=Input_Selection_Mask AND Assign_Port_Mask
                       Reset of event Port_Change_Event


B)                          TEMP1=0

              C)      N
                       TEMP2=TEMP1 AND Ports
     D)
                  Change_State=TEMP2 XOR Idle_State_Mask


       E)                 Change_State=0

          F)      N
                     Signaling of Port_Change_Event
```
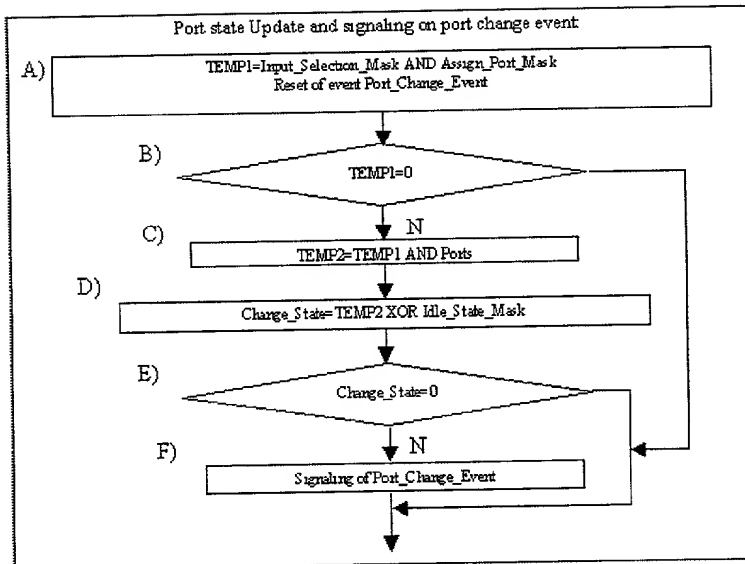
Fig 12 – Kernel – Port State Update

Task state Update

A) TCB_Pointer = FIRST_TCB_POINTER

B) Current_TCB Status = SUSPEND ?

C) TCB_Pointer = Current_TCB Next_TCB

D) TCB_Pointer <> NULL ?

E) Current_TCB.Status = READY ?

F) Current_TCB.Status = WAIT ?

G) ERROR

H) ECB_Pointer=FIRST_ECB_POINTER

I) Current_TCB.Event_ID = Current_ECB.Event_ID ?

J) Current_ECB.Control = ON ?

K) Current_TCB.Status=READY

L) ECB_Pointer=Current_ECB Next_ECB

M) ECB_Pointer <> NULL ?

N) ERROR

Y   N

Fig 13 – Kernel – Task State Update

A) `TCB_Pointer=FIRST_TCB_POINTER`

B)
```
Reset Max_Priority
Reset Task_ID_Winner
Reset Max_Wait_Time
```

C) Current_TCB Status = READY ?

Y

D) Current_TCB.Priority > Max_Priority ?

E)
```
Max_Priority=Current_TCB Priority
Task_ID_Winner=Current_TCB.Task_ID
Max_Wait_Time=Current_TCB.Wait_Time
```

N

F) Current_TCB.Priority = Max_Priority ?

Y

G) Current_TCB Wait_Time > Max_Wait_Time ?

Y

H)
```
Max_Wait_Time=Current_TCB Wait_Time
Task_ID_Winner=Current_TCB.Task_ID
```

I) `INC(Current_TCB.Wait_Time)`

J) `TCB_Pointer=Current_TCB Next_TCB`

K) TCB_Pointer <> NULL ?
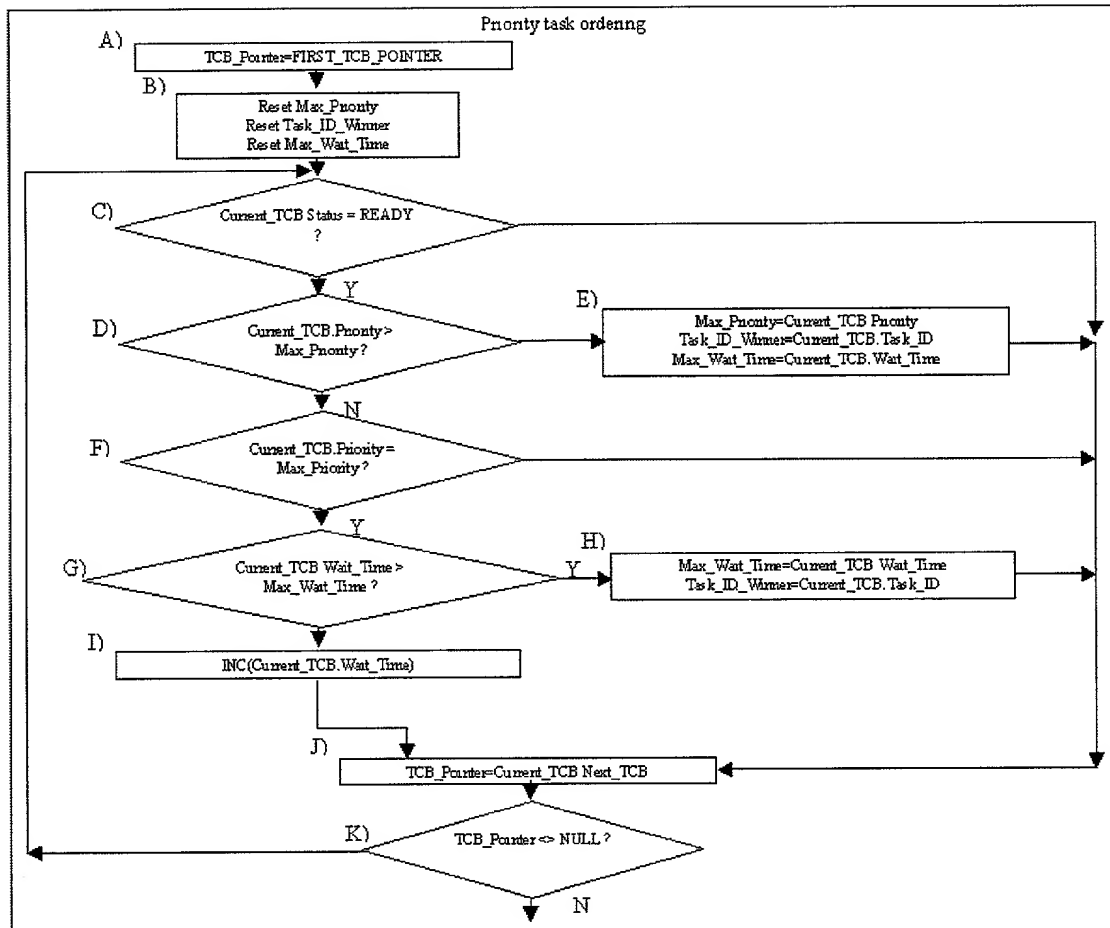
N

Fig 14 – Kernel – Priority Task Ordering

Context and control restore

A) Task_ID_Winner = NULL?

B) goto DISPATCHER

C) TCB_Pointer=FIRST_TCB_POINTER

N

D) Task_ID_Winner =
Current_TCB.Task_ID?

N

E) TCB_Pointer=Current_TCB.Next_TCB

F) TCB_Pointer <> NULL ?

N

G) ERROR

H) IP=Current_TCB.Task_Next_IP

I) Current_TCB.Status=ACTIVE

J) DMCB_Pointer=FIRST_DMCB_POINTER

K) Task_ID_Winner =
Current_DMCB.Task_ID ?

N

L) DMCB_Pointer=Current_DMCB.Next_DMCB

N) DMCB_Pointer <> NULL
?

N

O) ERROR

M) DM_Pointer=Current_DMCB.Data_Memory_Base_Address

P)
REG0=[DM_Pointer+REG0_OFFSET]
REG1=[DM_Pointer+REG1_OFFSET]
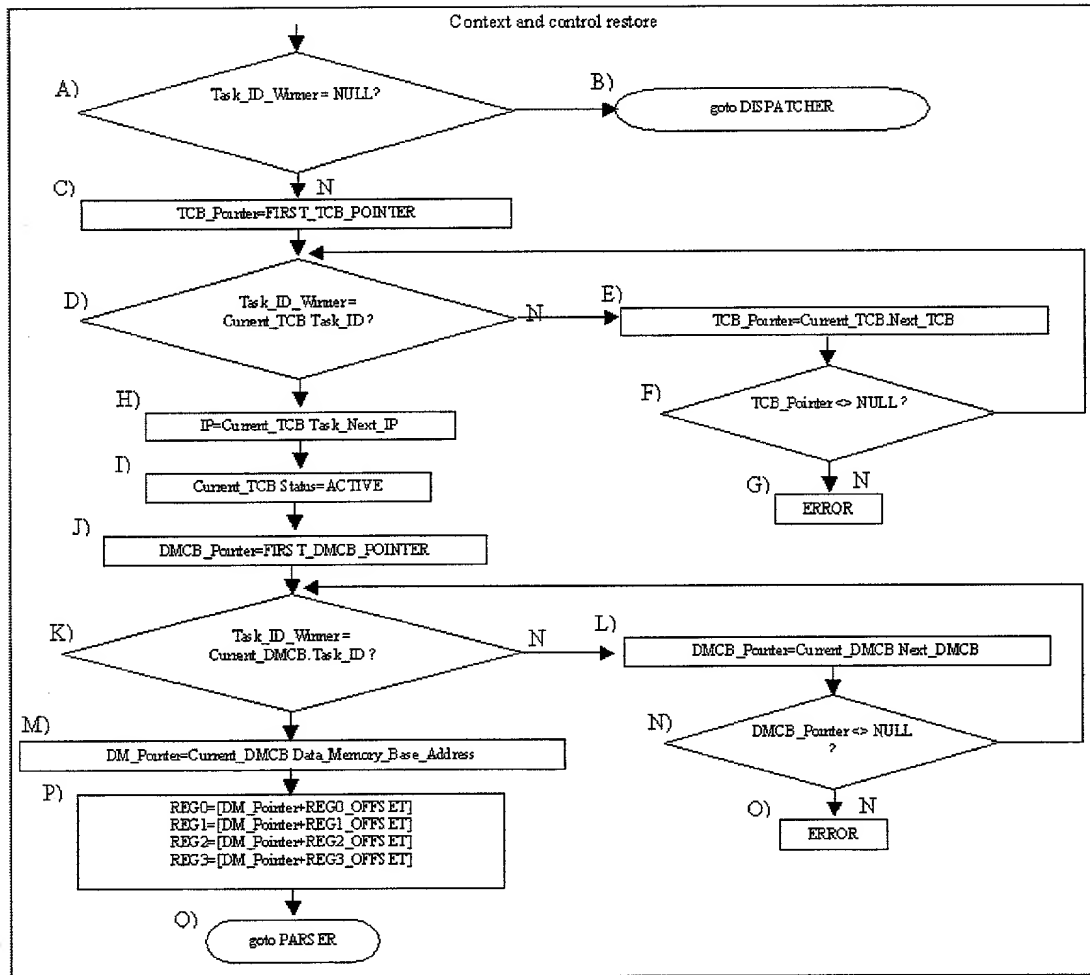REG2=[DM_Pointer+REG2_OFFSET]
REG3=[DM_Pointer+REG3_OFFSET]

O) goto PARSER

Fig 15 – Kernel – Context and Control Restore